

Sector Cache Optimizations for the K Computer

Swann Perarnau, Mitsuhisa Sato RIKEN AICS, University of Tsukuba

Sector Cache on the SPARCVIIIfx

- ► On-demand split of the shared L2 cache.
- ► User controlled mapping between accesses and sectors.
 - → Isolation of thrashing accesses.
 - → Select and keep useful data in cache.

Issues

- ► Low-level compile-time API.
- ► Hard to predict impact on performance.
- ► Little support from compiler and performance analysis tools.

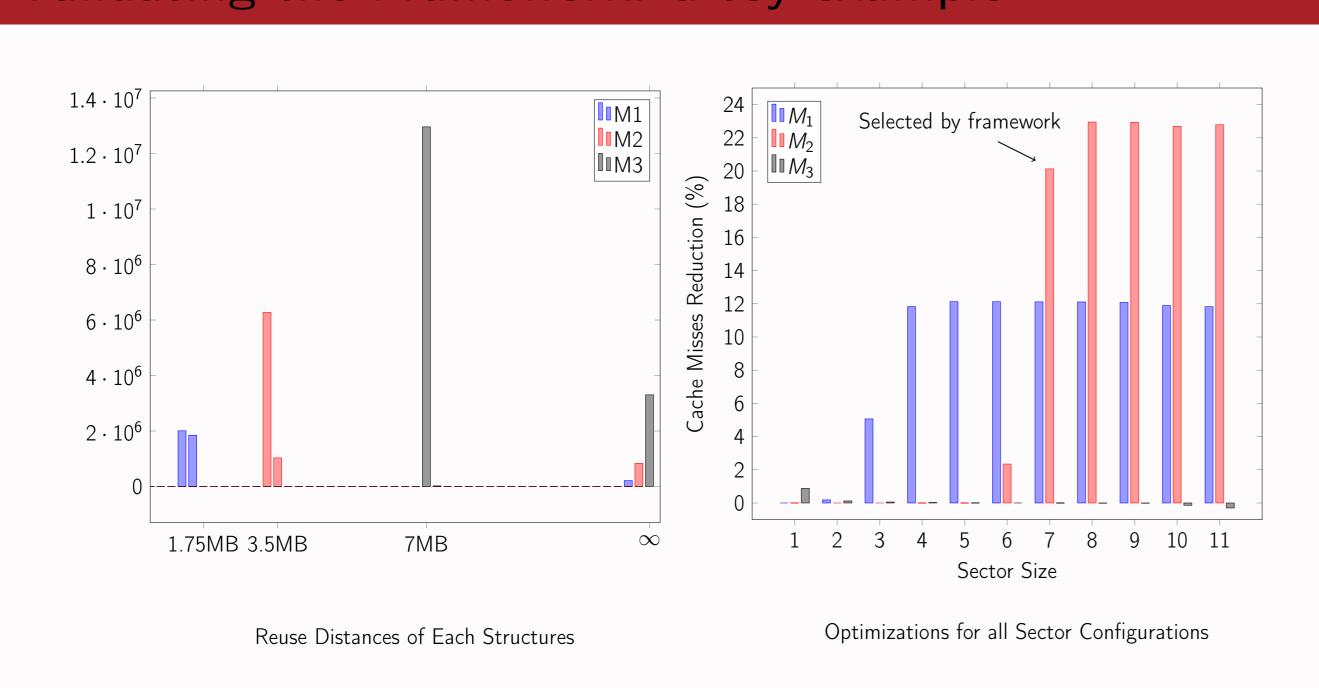
Current Sector Cache API

Locality Measurements

Reuse Distance: for a memory access, the number of unique memory locations touched since the previous access to the same location.

- → an architecture-independent measure closely related to the cache misses triggered by an application.
- \rightarrow use it to measure consequences of isolating one structure by itself with the sector cache.

Validating the Framework: a toy example



Our Goals

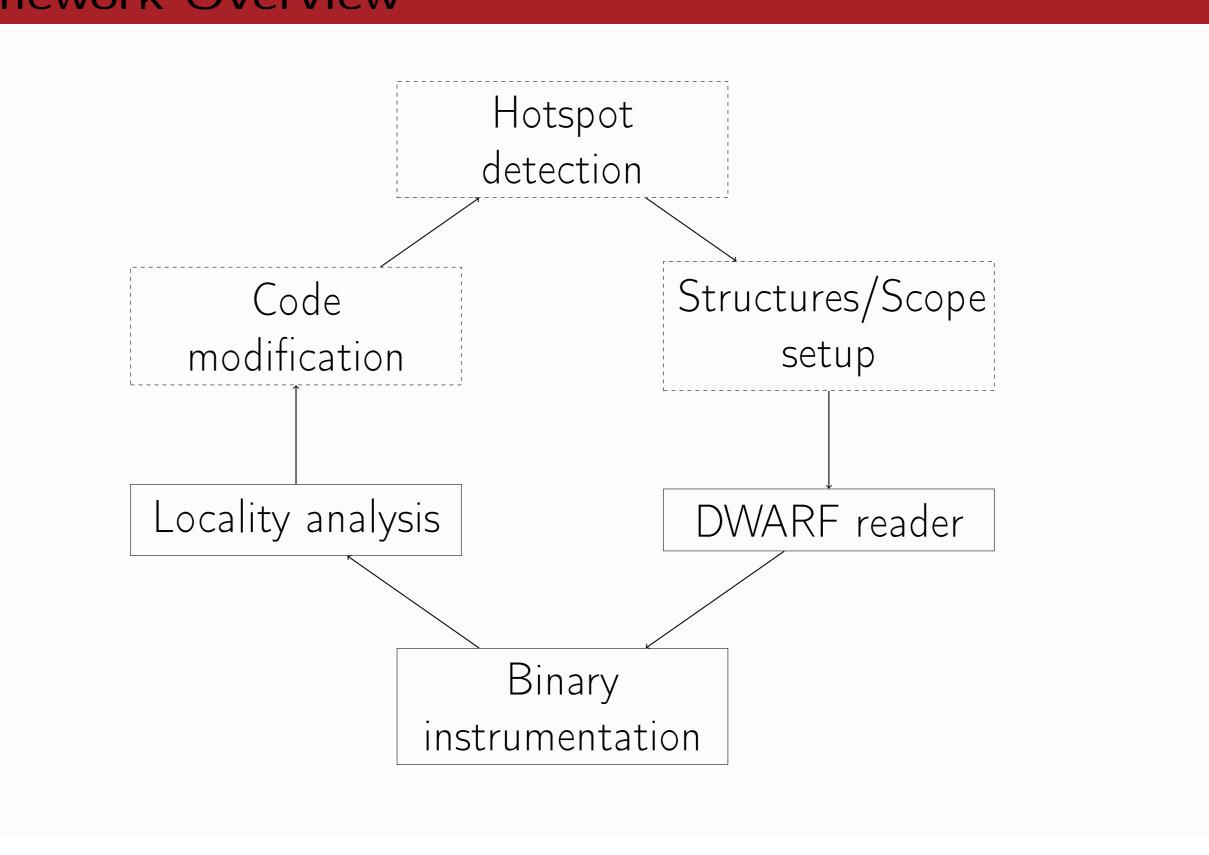
Assess applicability of the sector cache to optimize HPC applications.

- ► Study potential optimization strategies.
- ► Help users find good sector cache optimizations.
- ► Aim for as much automation as possible.

Results

- ▶ efficient cache optimization of classical HPC benchmarks.
- ► framework for locality analysis and optimization of HPC applications.
- ▶ on-going automation, already little user action required.

Framework Overview



Reuse exemple

Access :	Distance :		
load 0x10 load 0x20 load 0x30 load 0x10 load 0x20 load 0x10 load 0x30	∞ ∞ ∞ 2 2 1 2	Density	Distance

Optimizing the NAS Parallel Benchmarks

Benchmark	Function	Isolated Variables	Sector Size	Miss Reduction (%)	Runtime Reduction (%)
CG	conj_grad	р	(1,11)	19	10
LU	ssor	a,b,c,d	(2,10)	48	8
	blts	ldz,ldy,ld×,d		75	10
	buts	d,udx,udy,udz		18	3
	jacld	a,b,c,d		64	14
	jacu	a,b,c,d		57	6

Acknowledgements

Part of the results were obtained by early access to the K computer at the RIKEN AICS. This work was supported by the JSPS Grant-in-Aid for JSPS Fellows Number 24.02711.